HIGH POWER, HIGH EFFICIENCY PHEMTS FOR USE AT 8 GHZ

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ABSTRACT

Power PHEMTs from 4.8 mm to 14.4 mm gate periphery have been characterized at 8 GHz to study the effect of device scaling on output power, gain, and efficiency. The effect of unit gate width, gate to gate spacing, and substrate thickness on PHEMT performance is also described. A 14.4 mm device delivered 8.09 W with 12.67 dB associated gain and 55.8 % PAE under 8 V operation at 8 GHz.

INTRODUCTION

Considerable interest exists in developing large periphery power PHEMTs for use in communication and radar systems at frequencies up to K band. Amplifiers with 40 W at S-Band [1], 20 W at C-Band [2], 12.3 W at X-Band [3], and 4.7 W at K-Band [4] have been demonstrated by combining two or more of these devices. At 12 GHz, output powers as high as 6 W with 10.8 dB associated gain and 52 % PAE have been measured from a single 8 mm PHEMT device at 9 V drain bias [5]. In this paper, we discuss device considerations including substrate thickness, gate to gate spacing, and unit gate width, and demonstrate how device performance scales at 8 GHz with increasing periphery.

DEVICE CHARACTERISTICS

Devices with gate peripheries ranging from 1.2 mm to 16.8 mm were fabricated on the same mask set using standard e-beam defined 0.25 μm tri-layer T-gates. Conventional mesa technology was used to define the active areas followed by deposition of NiAuGe to form alloyed ohmic contacts. Gate recessing was performed using both wet and dry etching techniques with TiPtAu being used as the gate metal. Additional discussion of the material structure can be found in reference [6].

Substrate thickness

3 mm and 3.2 mm devices were used to study the effects of substrate thickness on device performance at 8 GHz. Substrate thicknesses of 2 mil (50 μm) and 4 mil (100 μm) were processed. A substrate thickness of 2 mils allows devices to have individually grounded source vias which lowers the source inductance, resulting in higher gain. The devices processed on the 4 mil wafer, depicted in figure 1a, are 0.25 μm PHEMTs with a total of 14 gate fingers and a unit gate width of 215 μm. The devices processed on the 2 mil substrate, shown in figure 1b, are 0.25 μm PHEMTs with a total of 16 gate fingers and a unit gate width of 200 μm. RF performance for both style devices is compared in figure 2. The most notable difference in device

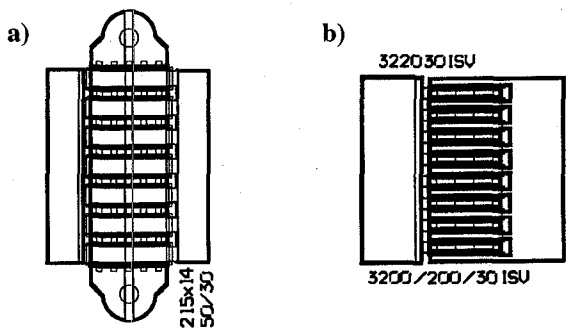

Figure 1: a) 3 mm PHEMT layout with end vias processed on 4 mil GaAs. b) 3.2 mm PHEMT layout using individually grounded source vias processed on 2 mil GaAs.

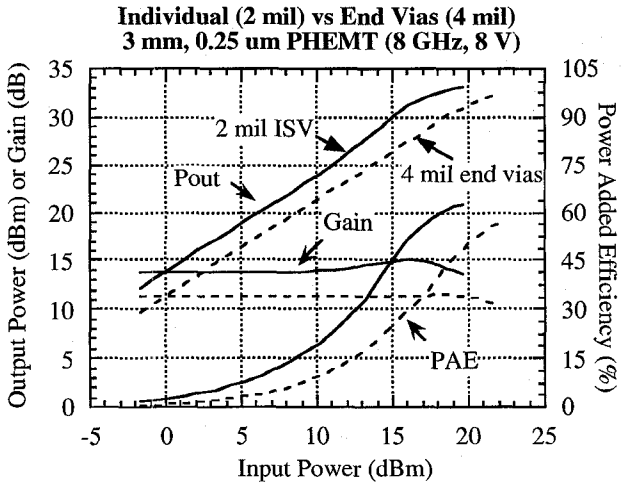

Figure 2: Power performance of the PHEMTs shown in figure 1. 2 mil performance is solid. 4 mil performance is dashed.

performance is a 2.5 dB improvement in gain at power for the device processed with individually grounded source vias (i.e. 2 mil wafer). Based on these results, all remaining devices were fabricated on 2 mil substrates with individually grounded source vias.

Unit gate width

3.2 and 3.3 mm PHEMTs with 100, 150 and 200 μm unit gate widths were measured at 8 GHz. These devices had 30 μm gate to gate spacing and utilized 2 mil thick GaAs. It is well known that as the unit gate width increases, device gain decreases due to an increase in gate resistance and phasing mismatches caused by the distributed nature of the gate and drain lines. Several devices were measured for each gate width, as shown in figure 3. Device gain decreases by 2.3 dB when the unit gate width increases from 100 to 200 μm. Output power and power added efficiency (PAE) is relatively unchanged.

Gate to Gate spacing

3 mm devices with 30 and 40 μm gate to gate spacing (100 and 150 μm unit gate width) were measured at 8 GHz. No noticeable difference in output power, gain, or efficiency was observed for a given unit gate width.

Based on the measured results for the 3 mm devices, we chose to study the scaling properties of PHEMTs processed using individually grounded source vias, 150 μm unit gate width, and 30 μm gate to gate spacing.

RESULTS AND DISCUSSION

In order to evaluate the power performance of large periphery devices (4.8 to 14.4 mm), jigs were designed with appropriate matching structures and bias networks, as shown in figure 4. Techniques similar to those described in [6] were used. Load pull measurements and small signal models for 3 mm devices were scaled to design the matching networks. 15 mil Alumina substrates provide a match from 50 ohms to 20 ohms at the input and output. A 5 mil K38 substrate is used to complete the input transformation. On the output, 5 mil Alumina is used to transform the drain impedance to 20 ohms. All bias networks and DC blocking capacitors are included on the jigs. Three jigs were designed to cover device peripheries from 4.8 to 14.4 mm. Input and output losses of 0.5 dB were measured and removed from all measurements to de-embed the data to the device terminals.

4.8, 8.4 and 14.4 mm devices were mounted on carriers and bonded into the jigs for CW microwave power testing. Output power, gain, and efficiency were measured as a function of input power. Measured results are shown in figures 5a, 5b, and 5c. The 4.8 mm device produced 3.25 W with an associated gain of 14.15 dB and 58.7% PAE at a drain voltage of 8 V and associated current of 665 mA. The 8.4 mm device produced 5.08 W with an associated gain of 13.61 dB and 56.8% PAE at a drain voltage of 8 V and associated current of 1072 mA. The 14.4 mm device produced 8.09 W with an associated gain of 12.67 dB and 55.8% PAE at a drain voltage of 8V and associated current of 1721 ma. Assuming a thermal resistivity of 60 °C-mm/W (based on 4 mil GaAs device data), the channel temperature rise is less than 30 °C when the devices are operated at power.

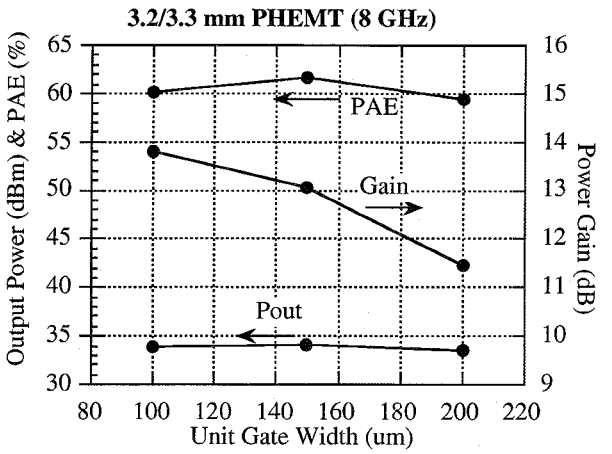

Figure 3: Effect of unit gate width on 3 mm PHEMT performance at 8V. Devices use 2 mil GaAs substrates and have 0.25 μm gates with 30 μm gate to gate spacing.

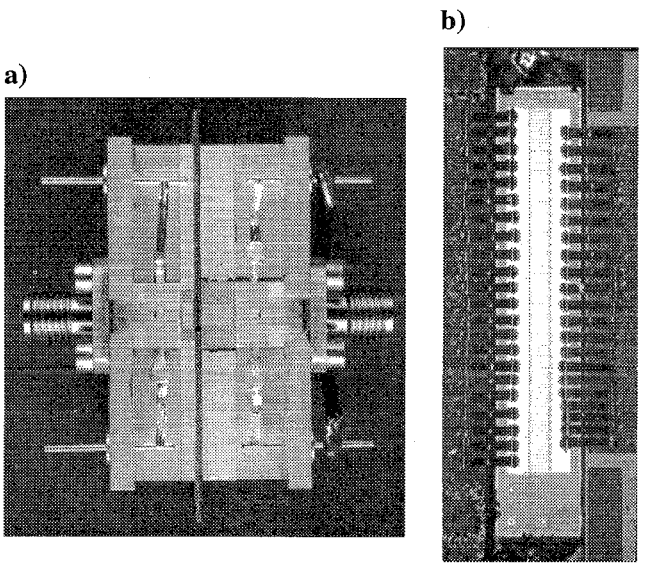

Figure 4: a) 8 GHz power tuning jig for 14.4 mm PHEMTs. b) Close up view of 14.4 mm PHEMT.

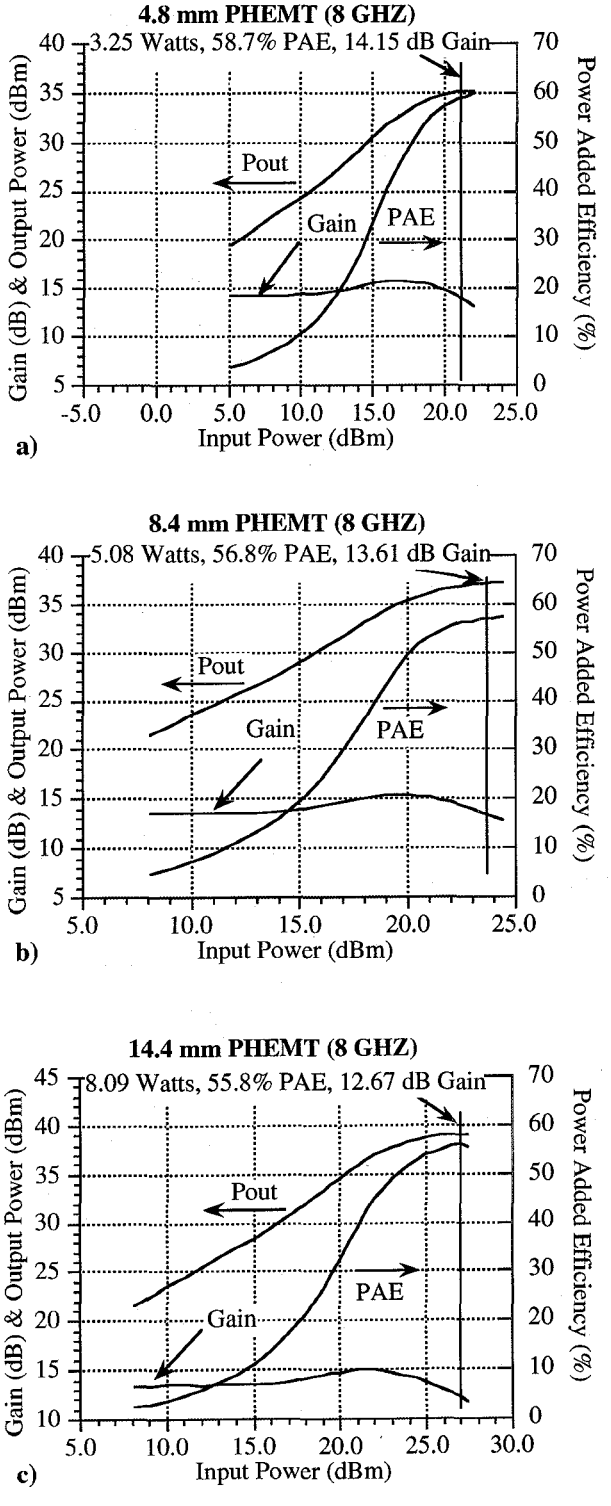

Figure 5: 8 GHz power performance at V_{ds}=8V for PHEMTs with 0.25 μm gates, 150 μm unit gate widths, and 30 μm gate to gate spacing. 0.5 dB input and 0.5dB output jig loss removed from data. a) 4.8 mm, b) 8.4 mm, c) 14.4 mm.

Table 1: PHEMT Scaling (8 GHz)

periphery (mm)	P_{out} (W)	G_p (dB)	PAE (%)	V_{ds} (V)	I_{ds} (mA)
4.8	3.25	14.15	58.7	8.0	665
8.4	5.08	13.61	56.8	8.0	1072
14.4	8.09	12.67	55.8	8.0	1721

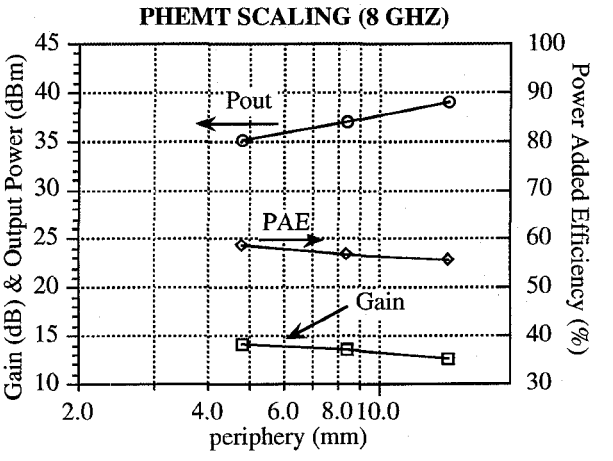

Figure 6: Effect of periphery on PHEMT performance at 8 GHz for the devices described in figure 5.

The effect of device scaling from 4.8 to 14.4 mm is shown in figure 6 and tabulated in table 1. Gain and PAE decrease only slightly as the periphery increases. Output power increases at a rate of 2.5 dB per doubling of periphery, power gain decreases at a rate of 0.9 dB per doubling, and PAE decreases at a rate of 1.8 percentage points per doubling. The excellent results obtained to date suggest that further scaling, with corresponding high gain and efficiency, may be possible.

CONCLUSION

Device considerations including substrate thickness, unit gate width, gate to gate spacing, and periphery were discussed. Using individually grounded source vias instead of conventional side vias (2 mil vs 4 mil substrate) was found to improve device gain by about 2.5 dB at 8 GHz. There was also a 2.3 dB increase in power gain when the unit gate width was decreased from 200 to 100 μm. PHEMTs with 150 μm unit gate width were successfully scaled to 14.4 mm while maintaining reasonable efficiency and gain, making these devices excellent candidates for high power X-band solid state amplifiers.

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